ABSTRACT

Reducing power consumption has become a key goal for system-on-a-chip (SOC) designs. Fast and accurate power estimation is needed early in the design process, since power reduction methods tend to have greater impact at higher abstraction levels. Unfortunately, current approaches to power estimation, which concentrate on the register transfer-level of abstraction or lower, require long computing times. Higher-level approaches, while faster, may suffer from inaccuracy. However, the advent of cores enables a hybrid approach that yields fast and accurate estimates from high-level models. In particular, we use power estimation data obtained from the gate-level for a core's representative input stimuli data (instructions), and we propagate this data to a higher (object-oriented) system-level model, which is parameterizable and executable. Depending on the kind of cores, various parameterizable look-up table techniques are used to facilitate self-analyzing core models. As a result, our technique is orders of magnitudes faster than gate-level power estimation techniques and features an accuracy that is suited to make reliable power-related system-level design decisions.